SONY

CXA3135AN

All Band TV Tuner IC with On-chip PLL

Description

The CXA3135AN is a monolithic TV tuner IC which integrates local oscillator and mixer circuits for VHF band, local oscillator and mixer circuits for UHF band, an IF amplifier and a tuning PLL onto a single chip, enabling further miniaturization of the tuner. The PLL on this IC supports the I^2C bus format.

Features

- Low noise figure
- Low power consumption (5 V, 54 mA typ.)
- On-chip tuning PLL (I^2C bus format)
- Selection of frequency steps 31.25 kHz, 50 kHz and 62.5 kHz
- On-chip 4-output band switch

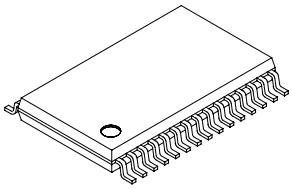
Applications

- TV tuners
- VCR tuners
- CATV tuners

Structure

Bipolar silicon monolithic IC

30 pin SSOP (Plastic)



Absolute Maximum Ratings (Ta = 25 °C)

• Supply voltage	$V_{CC}1, V_{CC}2$	–0.3 to +5.5	V
	$V_{CC}3$	–0.3 to +10.0	V
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation	P_D	880	mW
	(when mounted on a substrate)		

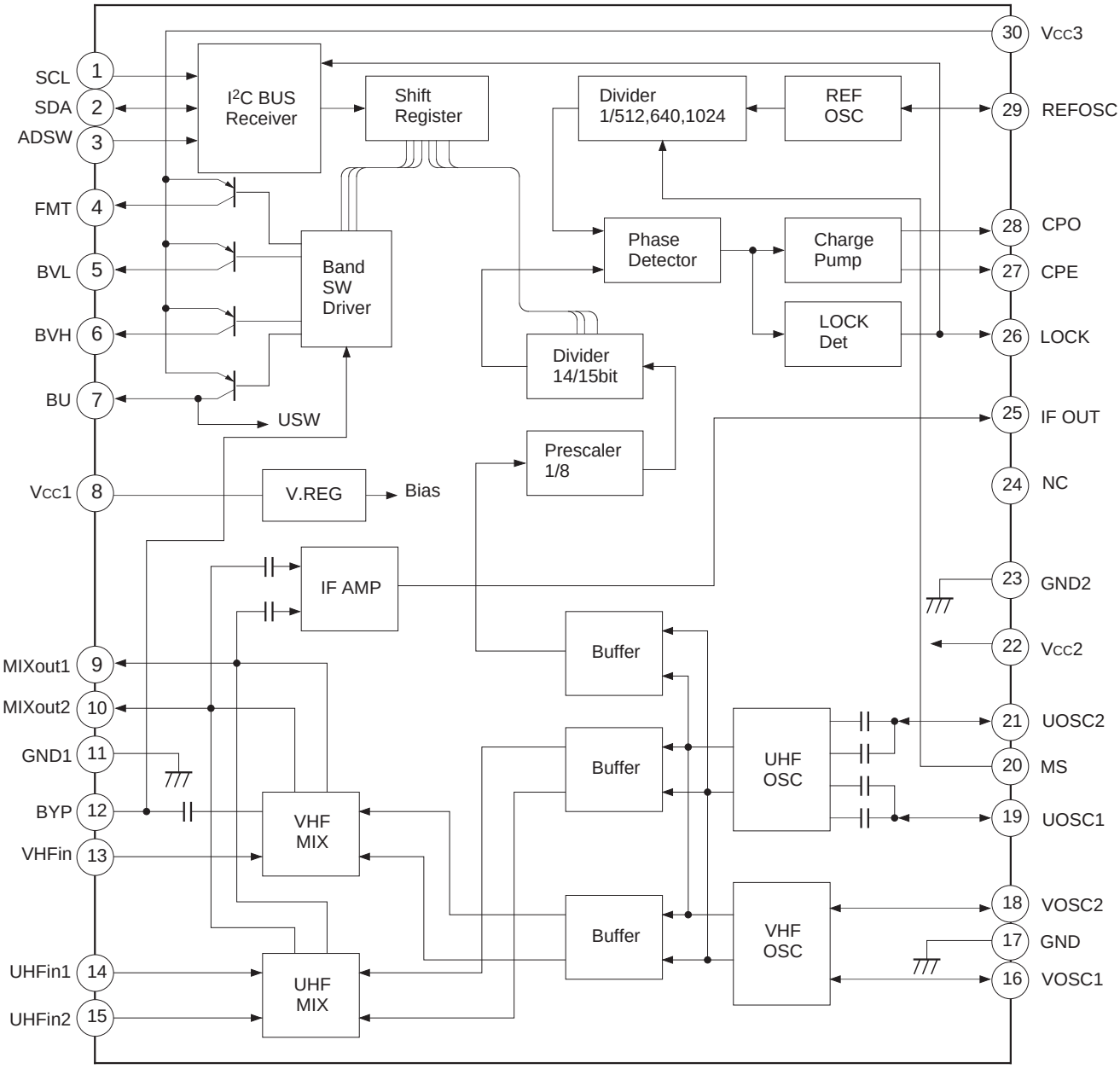
Operating Conditions

• Supply voltage	$V_{CC}1, V_{CC}2$	4.75 to 5.30	V
	$V_{CC}3$	4.75 to 9.45	V
• Operating temperature	Topr	–25 to +75	°C

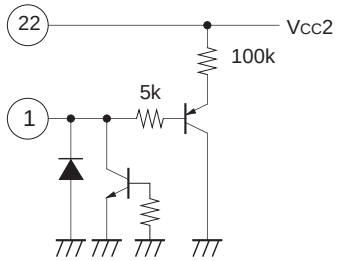
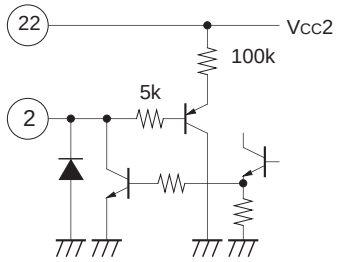
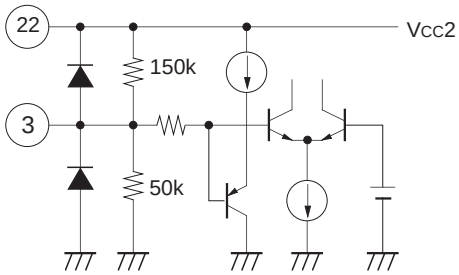
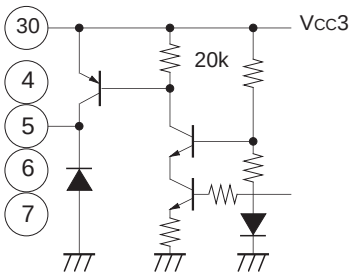
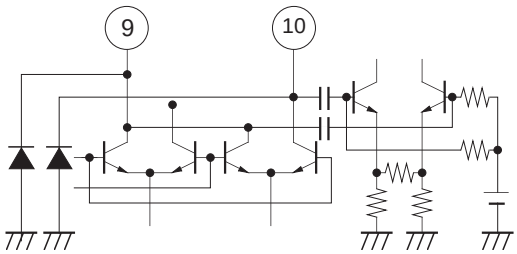
Note) Electrostatic discharge strength is weak, and care should be taken in handling this IC.

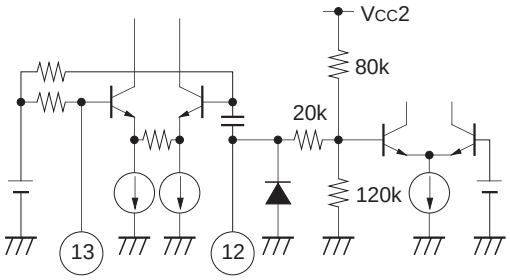
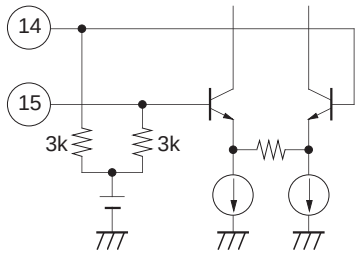
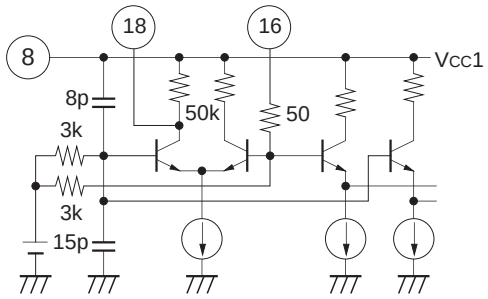
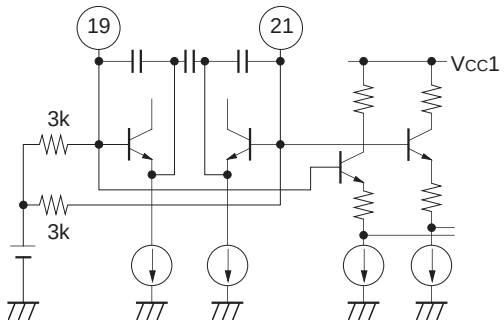
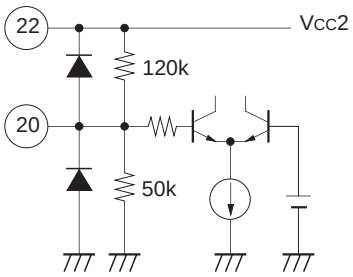
E97759-TE

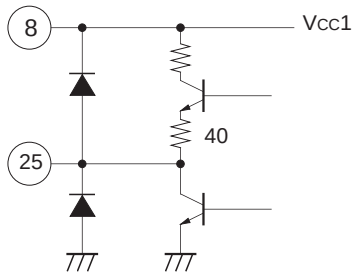
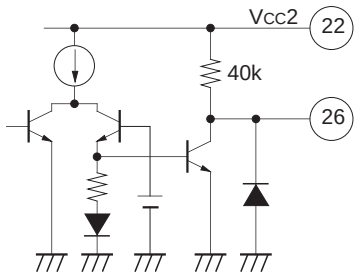
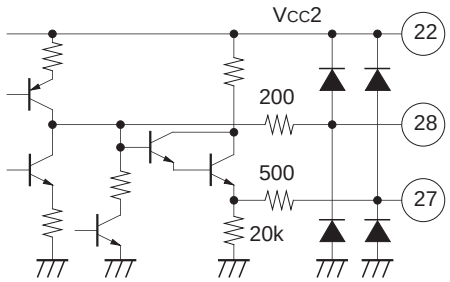
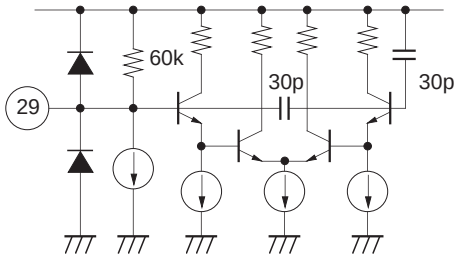
Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	Equivalent circuit	Pin voltage (V)	Description
1	SCL		—	Clock input.
2	SDA		—	Data I/O.
3	ADSW		1.25 (when open)	Address selection. This pin controls bits 2 and 1 of the address byte.
4	FMT		ON : 4.9 OFF : 0	4 : Output for FM TRAP. 5 : Power supply output for VL band. 6 : Power supply pin for VH band. 7 : Power supply output for UHF band. The pin corresponding to the selected band goes High.
5	BVL			
6	BVH			
7	BU			
8	Vcc1			Analog circuit power supply.
9	MIXout1			Mixer outputs.
10	MIXout2			
11	GND1	—	—	Analog circuit GND.

Pin No.	Symbol	Equivalent circuit	Pin voltage (V)	Description
12	BYP		3.0 (when open)	VHF input GND and FMT/BU data switching.
13	VHFin		2.3 (VHF) 0 (UHF)	VHF input. The input format is unbalanced input.
14	UHFin1		0 (VHF) 2.3 (UHF)	UHF inputs. The input method can be selected from balanced input or unbalanced input.
15	UHFin2		0 (VHF) 2.3 (UHF)	
16	VOSC1		3 (VHF) 3.1 (UHF)	External resonance circuit connection for VHF oscillator.
18	VOSC2		4.0 (VHF) 5.0 (UHF)	
17	GND		—	GND
19	UOSC1		3.2 (VHF) 2.9 (UHF)	External resonance circuit connection for UHF oscillator.
21	UOSC2		3.2 (VHF) 2.9 (UHF)	
20	MS		1.5 (when open)	Frequency step mode selection. Five modes can be selected according to the applied voltage.

Pin No.	Symbol	Equivalent circuit	Pin voltage (V)	Description
22	Vcc2	—	—	PLL circuit power supply.
23	GND2	—	—	PLL circuit GND.
24	NC	—	—	No connected.
25	IFOUT		2.3	IF output.
26	LOCK		5.0 (Lock) 0.2 (UNLock)	LOCK detection. High when locked, Low when unlocked.
27	CPE		0.6	NPN transistor connection for varicap diode drive.
28	CPO		2.0	Charge pump output. Connect a loop filter.
29	REFOSC		4.3	Crystal connection for reference oscillator.
30	Vcc3		—	Power supply for external supply.

Electrical Characteristics See the Electrical Characteristics Measurement Circuit.

Circuit Current (V_{CC}=5 V, Ta=25 °C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Circuit current A	AI_{CCV}	V_{CC}1 current, Band switch output open during VHF operation	30	41	55	mA
	AI_{CCU}	V_{CC}1 current, Band switch output open during UHF operation	31	42	56	mA
Circuit current D	DI_{CC}	V_{CC}2 current	7	11	15	mA

OSC/MIX/IF Amplifier Block

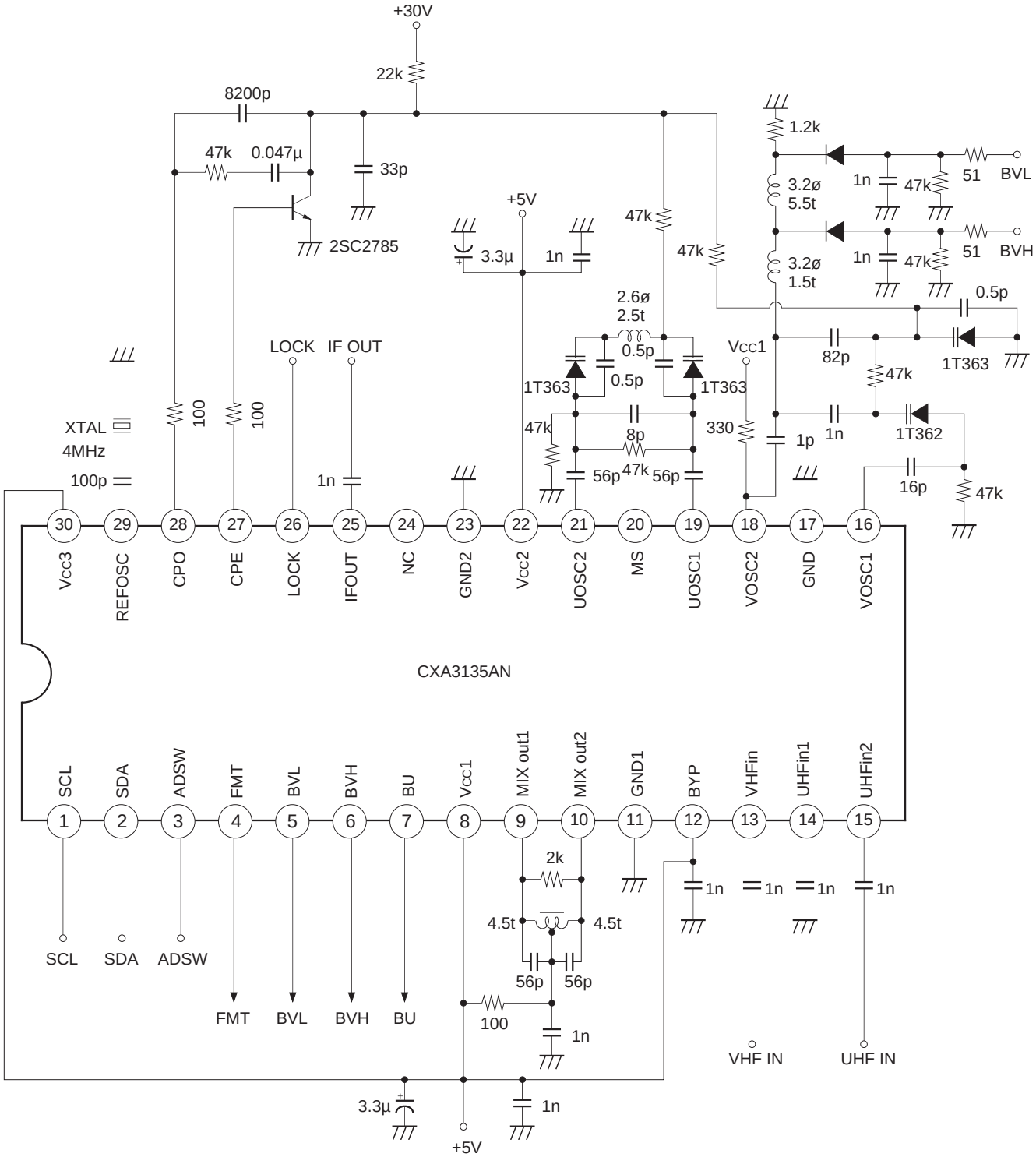
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Conversion gain *1	CG1	VHF operation f_{RF} = 55 MHz	21	24	27	dB
	CG2	VHF operation f_{RF} = 360 MHz	22	25	28	dB
	CG3	UHF operation f_{RF} = 360 MHz	26	29	32	dB
	CG4	UHF operation f_{RF} = 800 MHz	27	30	33	dB
Noise figure *1, *2	NF1	VHF operation f_{RF} = 55 MHz		12	15	dB
	NF2	VHF operation f_{RF} = 360 MHz		11	14	dB
	NF3	UHF operation f_{RF} = 360 MHz		8.5	12.5	dB
	NF4	UHF operation f_{RF} = 800 MHz		9.5	13.5	dB
1 % cross modulation *1, *3	CM1	VHF operation f_D = 55 MHz, f_{UD} = ±12 MHz	97	101		dBµ
	CM2	VHF operation f_D = 360 MHz, f_{UD} = ±12 MHz	96	100		dBµ
	CM3	UHF operation f_D = 360 MHz, f_{UD} = ±12 MHz	92	96		dBµ
	CM4	UHF operation f_D = 800 MHz, f_{UD} = ±12 MHz	88	92		dBµ
Maximum output power	Pomax	50 Ω load saturation output	+5	+10		dBm
Switch ON drift *4	Δfsw1	VHF operation f_{OSC} = 100 MHz Δf from 3 s to 3 min after switch ON			±300	kHz
	Δfsw2	VHF operation f_{OSC} = 405 MHz Δf from 3 s to 3 min after switch ON			±400	kHz
	Δfsw3	UHF operation f_{OSC} = 405 MHz Δf from 3 s to 3 min after switch ON			±400	kHz
	Δfsw4	UHF operation f_{OSC} = 845 MHz Δf from 3 s to 3 min after switch ON			±500	kHz
Supply voltage drift *4	Δfst1	VHF operation f_{OSC} = 100 MHz Δf when V_{CC} 5 V changes ±5 %			±150	kHz
	Δfst2	VHF operation f_{OSC} = 405 MHz Δf when V_{CC} 5 V changes ±5 %			±250	kHz
	Δfst3	UHF operation f_{OSC} = 405 MHz Δf when V_{CC} 5 V changes ±5 %			±200	kHz
	Δfst4	UHF operation f_{OSC} = 845 MHz Δf when V_{CC} 5 V changes ±5 %			±250	kHz

*1 Measured value for untuned inputs.
*2 Noise figure is the direct-reading value of NF meter in DSB.
*3 Desired signal (f_D) input level is –30 dBm. Undesired signal (f_{UD}) is 100 kHz, 30 % AM at ±12 MHz.
The measurement value is undesired signal level, it measured with a spectrum analyzer at S/I=46 dB.
*4 Value when the PLL is not operating.

PLL Block

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
SDA, SCL						
"H" level input voltage	V_{IH}		3		V_{CC}	V
"L" level input voltage	V_{IL}		GND		1.5	V
"H" level input current	I_{IH}	$V_{IH} = V_{CC}$		0	–0.1	µA
"L" level input current	I_{IL}	V_{IL} = GND		–1	–2	µA
SDA "L" output voltage	L_{SDA}	Sink current = 3 mA			0.4	V
Clock input hysteresis	CI_{HYS}		0.25	0.4	0.65	V
Clock rate	CI_{RATE}				0.5	MHz
CPO (charge pump)						
Output current 1	$I_{CPO}1$	Byte4/Bit6 = 0	±35	±50	±75	µA
Output current 2	$I_{CPO}2$	Byte4/Bit6 = 1	±140	±200	±300	µA
Leak current 1	LeakCP1	Byte4/Bit6 = 0			30	nA
Leak current 2	LeakCP2	Byte4/Bit6 = 1			100	nA
REFOSC						
Oscillator frequency range	F_{XTOSC}		3		12	MHz
Input capacitance	C_{XTOSC}		17.5	19	20.5	pF
Drive level	V_{XTOSC}		200	400		mVp-p
BVL, BVH, BU (Band SW)						
Output current	$I_{BS}1$	When ON			–25	mA
Saturation voltage	$V_{SAT}1$	When ON Sink current = 20 mA		100	200	mV
Leak current	LeakBS1	When OFF		0.5	3	µA
FMT (Band SW)						
Output current	$I_{BS}2$	When ON			–7	mA
Saturation voltage	$V_{SAT}2$	When ON Sink current = 5 mA		75	150	mV
Leak current	LeakBS2	When OFF		0.03	0.1	µA
Bus timing						
SCL clock frequency	f_{SCL}		0		400	kHz
Start waiting time	t_{WSTA}	See Timing Chart on Page 15.	1300			ns
Start hold time	t_{HSTA}	See Timing Chart on Page 15.	600			ns
Low hold time	t_{LOW}	See Timing Chart on Page 15.	1300			ns
High hold time	t_{HIGH}	See Timing Chart on Page 15.	600			ns
Start setup time	t_{SSTA}	See Timing Chart on Page 15.	600			ns
Data hold time	t_{HDAT}	See Timing Chart on Page 15.	1300			ns
Data setup time	t_{SDAT}	See Timing Chart on Page 15.	600			ns
Rise time	t_R	See Timing Chart on Page 15.			300	ns
Fall time	t_F	See Timing Chart on Page 15.			300	ns
Start setup time	t_{SSTO}	See Timing Chart on Page 15.	600			ns

Electrical Characteristics Measurement Circuit



Description of Functions

The CXA3135AN is a terrestrial wave broadcast tuner IC which converts frequencies to IF in order to tune and detect only the desired reception frequency of VHF, CATV and UHF band signals.

In addition to the mixer, local oscillator and IF amplifier circuits required for frequency conversion to IF, this IC also integrates a PLL circuit for local oscillator frequency control onto a single chip.

The functions of the various circuits are described below.

1. Mixer circuit

This circuit outputs the frequency difference between the signal input to VHFIN or UHFIN and the local oscillation signal.

2. Local oscillator circuit

A VCO is formed by externally connecting an LC resonance circuit composed of a varicap diode and inductance.

3. IF amplifier circuit

This circuit amplifies the mixer IF output, and consists of an amplifier stage and low impedance output stage.

4. PLL circuit

This PLL circuit fixes the local oscillator frequency to the desired frequency. It consists of a prescaler, main divider, reference divider, phase comparator, charge pump and reference oscillator. The control format supports the I^2C bus format. The following five modes can be selected according to the combination of the frequency division values of the main and reference dividers.

Mode	Main divider	Reference divider
B-0	15 bit	1024 fixed
B-1	14 bit	512 fixed
B-2	15 bit	640 fixed
B-3	15 bit	512 fixed
B-4	15 bit	512/1024 switching

Description of Analog Block Operation

(See the Electrical Characteristics Measurement Circuit.)

VHF oscillator circuit

- This circuit is a differential amplifier type oscillator circuit.
  Pin 18 is the output and Pin 16 is the input.
  Oscillation is performed by connecting an LC resonance circuit including a varicap to Pin 18 via coupled capacitance, inputting to Pin 16 with feedback capacitance, and applying positive feedback.
- Pin 18 is an open collector, so power must be supplied via the resonance circuit inductance or by the resistance or microinductor. The electric potential of Pin 18 at this time must be DC 3.5 V or more.
- The amplifier between Pins 16 and 18 has an extremely high gain. Therefore, care should be taken to avoid creating parasitic capacitance, resistance or other feedback loops as this may produce abnormal oscillation.

VHF mixer circuit

- The mixer circuit employs a double balance mixer with little local oscillation signal leakage.
  The input format is base input type, with Pin 12 grounded and the RF signal input to Pin 13.
- The RF signal is inserted from the oscillator, converted to IF frequency and output from Pins 9 and 10.
- Pins 9 and 10 are open collectors, so power must be supplied externally. The electric potential of Pins 9 and 10 at this time must be DC 4.0 V or more.

UHF oscillator circuit

- This oscillator circuit is designed so that two collector ground type Colpitts oscillators perform differential oscillation operation via an LC resonance circuit including a varicap. An LC resonance circuit including a varicap is connected between Pins 19 and 21.
- This circuit contains resonance capacitance comprising Colpitts oscillators, so the LC resonance circuit connected to Pins 19 and 21 oscillates at the frequency indicating the inductance characteristics.

UHF mixer circuit

- This circuit employs a double balance mixer like the VHF mixer circuit.
  The input format is base input type, with Pins 14 and 15 as the RF input pins. The input method can be selected from balanced input consisting of differential input to Pins 14 and 15 or unbalanced input consisting of grounding Pin 14 via a capacitor and input to Pin 15.
- Pins 9 and 10 are the mixer outputs.
- Pins 9 and 10 are open collectors, so power must be supplied externally. The electric potential of Pins 9 and 10 at this time must be DC 4.0 V or more.

IF amplifier circuit

- The signals frequency converted by the mixer are output from Pins 9 and 10, and at the same time are AC coupled inside the IC and input to the IF amplifier.
- Single-tuned filters are connected to Pins 9 and 10 in order to improve the interference characteristics of the IF amplifier.
- The signal amplified by the IF amplifier is output from Pin 25.
  The output impedance is approximately 75 Ω.

Description of PLL Block

The PLL on this IC supports the I²C bus control format. The control pins are as shown in the table below.

Symbol	Description
ADSW	Address selection
SCL	SCL input
SDA	SDA I/O

1) Mode Setting Method

The modes for each frequency step are set according to the MS pin voltage.

Mode	MS pin voltage	Main divider	Reference divider	Reference frequency	Frequency step*
B-0	0 to 0.15 Vcc	15 bit	1024	3.90625 kHz	31.25 kHz
B-1	OPEN	14 bit	512	7.8125 kHz	62.5 kHz
B-2	0.45 Vcc to 0.55 Vcc	15 bit	640	6.25 kHz	50 kHz
B-3	0.65 Vcc to 0.75 Vcc	15 bit	512	7.8125 kHz	62.5 kHz
B-4	0.85 Vcc to Vcc	15 bit	512/ 640/ 1024	7.8125 kHz/ 6.25 kHz/ 3.90625 kHz	62.5 kHz/ 50 kHz/ 31.25 kHz

* Frequency step is for when X'tal OSC = 4 MHz.

2) Address Setting

The responding address can be changed according to the ADSW pin voltage, so that multiple PLL can exist within one system.

Address

ADSW pin voltage	MA1	MA0
0 to 0.1 Vcc	0	0
OPEN or 0.2 Vcc to 0.3 Vcc	0	1
0.4 Vcc to 0.6 Vcc	1	0
0.9 Vcc to Vcc	1	1

3) Programming

The VCO lock frequency is obtained according to the following formula.

$fosc = fref \times 8 \times (32\ M + S)$

fosc : local oscillator frequency

fref : reference frequency

8 : prescaler fixed frequency division ratio

M : main divider frequency division ratio

S : swallow counter frequency division ratio

The variable frequency division ranges of M and S are as follows, and are set as binary.

$32 \leq M \leq 1023$ ($32 \leq M \leq 511$ for B-1 mode)

$0 \leq S \leq 31$

3-1) The normal control format is as follows.

3-1-1 : B-0/B-1/B-2/B-3 Modes

Write-mode : Slave Receiver

	MSB							LSB	
MODE	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
Address byte	1	1	0	0	0	MA1	MA0	0	A
Divider byte 1	0	M9*	M8	M7	M6	M5	M4	M3	A
Divider byte 2	M2	M1	M0	S4	S3	S2	S1	S0	A
Control byte	1	CP	T1	CD	X	X	X	OS	A
Band SW byte	X	X	X	X	BU	FMT	BVH	BVL	A

X : Don't care

* M9 is "0" for B-1 mode.

3-1-2 : B-4 Mode

Write-mode : Slave Receiver

	MSB							LSB	
MODE	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
Address byte	1	1	0	0	0	MA1	MA0	0	A
Divider byte 1	0	M9	M8	M7	M6	M5	M4	M3	A
Divider byte 2	M2	M1	M0	S4	S3	S2	S1	S0	A
Control byte	1	CP	T1	CD	X	R1	R0	OS	A
Band SW byte	X	X	X	X	BU	FMT	BVH	BVL	A

X : Don't care

3-2) The BU and FMT data order can be switched by DC grounding the BYP pin (VHF input ground side).

3-2-1 : B-0/B-1/B-2/B-3 Modes

Write-mode : Slave Receiver

	MSB							LSB	
MODE	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
Address byte	1	1	0	0	0	MA1	MA0	0	A
Divider byte 1	0	M9*	M8	M7	M6	M5	M4	M3	A
Divider byte 2	M2	M1	M0	S4	S3	S2	S1	S0	A
Control byte	1	CP	T1	CD	X	X	X	OS	A
Band SW byte	X	X	X	X	FMT	BU	BVH	BVL	A

X : Don't care

* M9 is "0" for B-1 mode.

3-2-2 : B-4 Mode

Write-mode : Slave Receiver

	MSB							LSB	
MODE	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
Address byte	1	1	0	0	0	MA1	MA0	0	A
Divider byte 1	0	M9	M8	M7	M6	M5	M4	M3	A
Divider byte 2	M2	M1	M0	S4	S3	S2	S1	S0	A
Control byte	1	CP	T1	CD	X	R1	R0	OS	A
Band SW byte	X	X	X	X	FMT	BU	BVH	BVL	A

X : Don't care

A : Acknowledge bit
MA0, MA1 : address setting
M0 to : main divider frequency division ratio setting
S0 to : swallow counter frequency division ratio setting
T1 : test mode selection (when "1")
CD : charge pump OFF (when "1")
OS : varicap output OFF (when "1")
CP : charge pump current switching (200 µA when "1", 50 µA when "0")
BVL : VL band switch control (output PNP Tr ON when "1")
BVH : VH band switch control (output PNP Tr ON when "1")
FMT : FM trap switch control (output PNP Tr ON when "1")
BU : UHF band switch control (output PNP Tr ON when "1")
R0, R1 : Reference divider frequency division ratio setting

Reference Divider Frequency Division Ratio Table

R1	R0	Reference divider
0	1	1024
1	1	512
X	0	640

X : Don't care

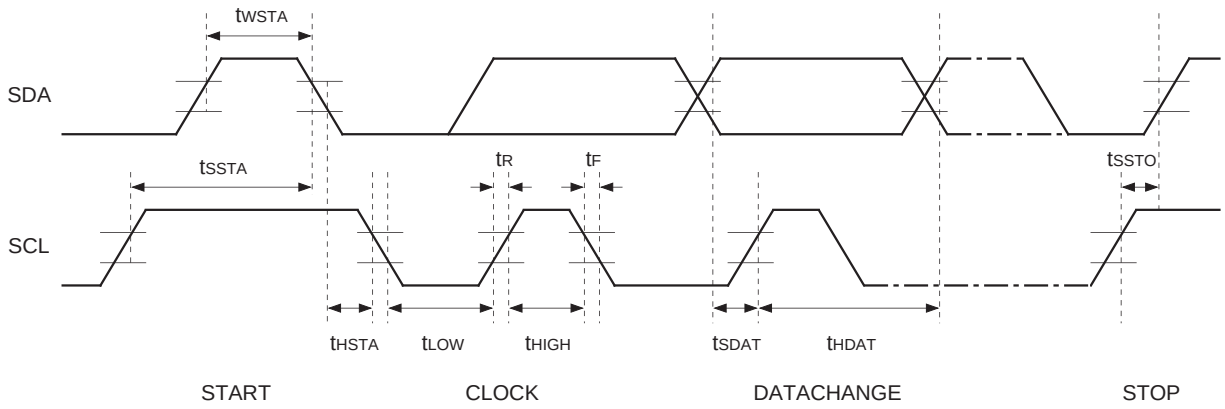
3-3) The read data format is as shown below.

Read-mode : Slave Transmitter

MODE	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
Address byte	1	1	0	0	0	MA1	MA0	1	A
Status byte	PR	FL	1	1	1	X	X	X	A

A : acknowledge bit
PR : power-on reset
FL : lock detection signal
MA0, MA1 : address setting

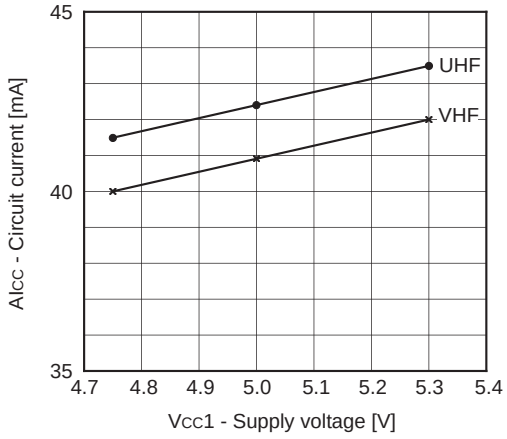
I²C Bus Timing Chart



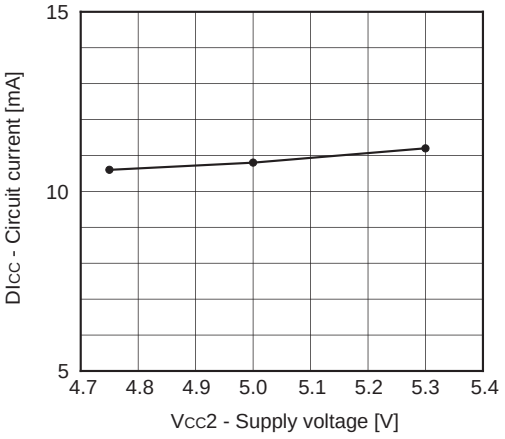
tSSTA =Start setup time
tWSTA =Start waiting time
tHSTA =Start hold time
tLOW =LOW clock pulse width
tHIGH =HIGH clock pulse width

tSDAT =Data setup time
tHDAT =Data hold time
tSSTO =Stop setup time
tR =Rise time
tF =Fall time

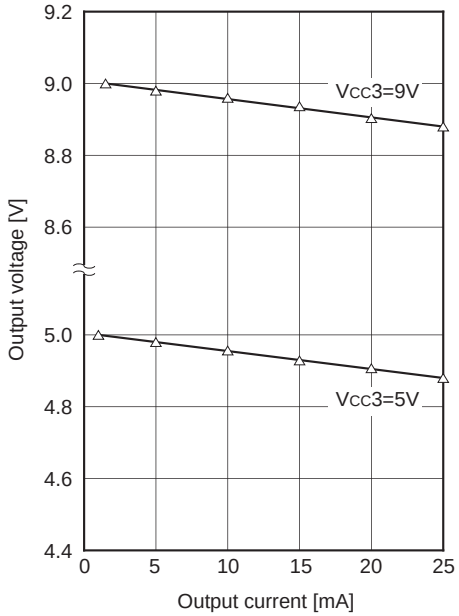
Circuit current vs. Supply voltage 1



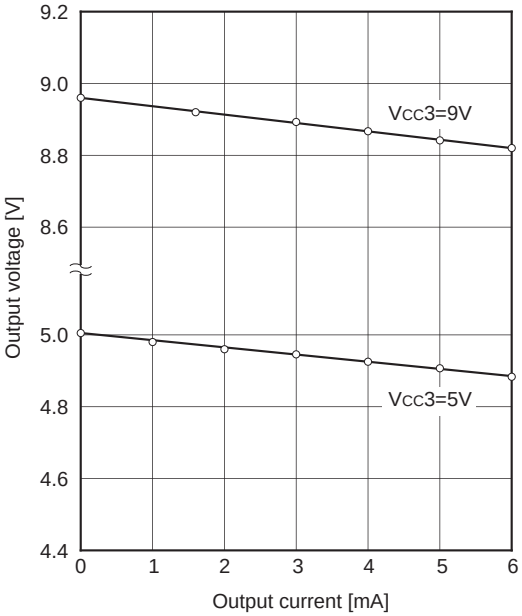
Circuit current vs. Supply voltage 2



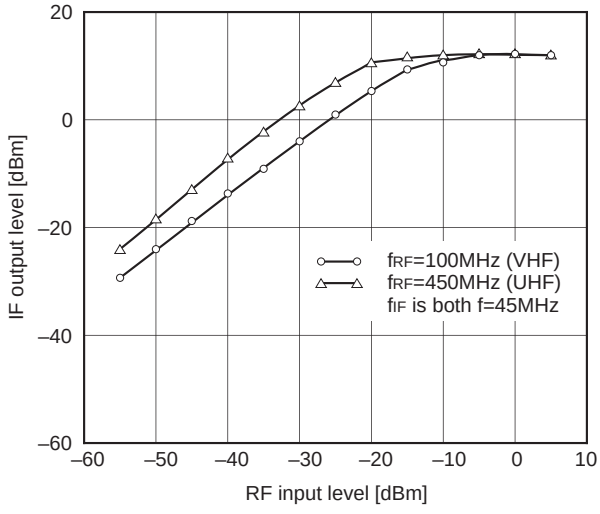
Band SW output voltage vs. Output current (BU, BVH, BVL)



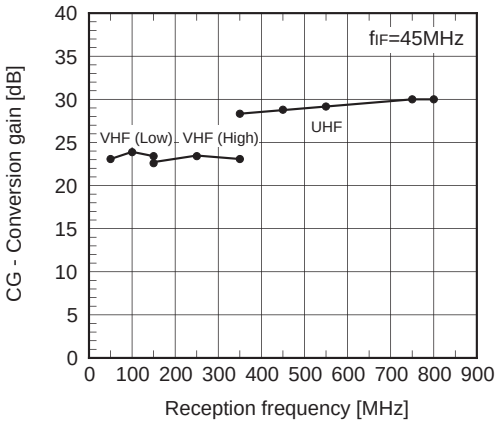
Band SW output voltage vs. Output current (FMT)



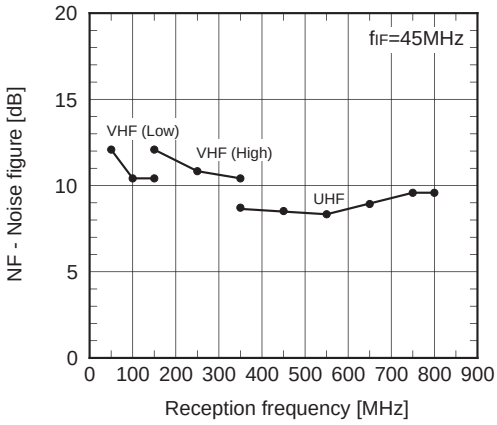
I/O characteristics (Untuned input)



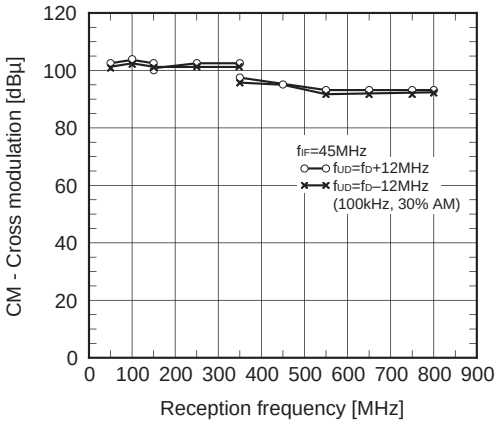
Conversion gain vs. Reception frequency (Untuned input)



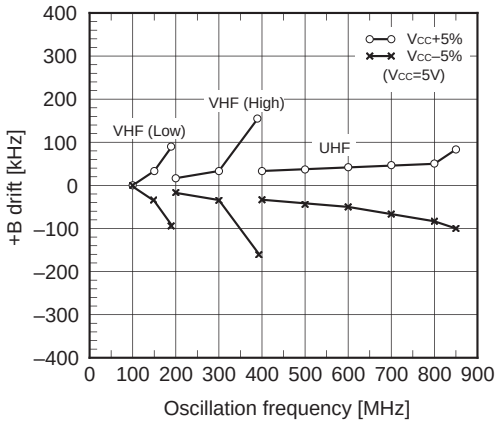
Noise figure vs. Reception frequency (Untuned input, in DSB)



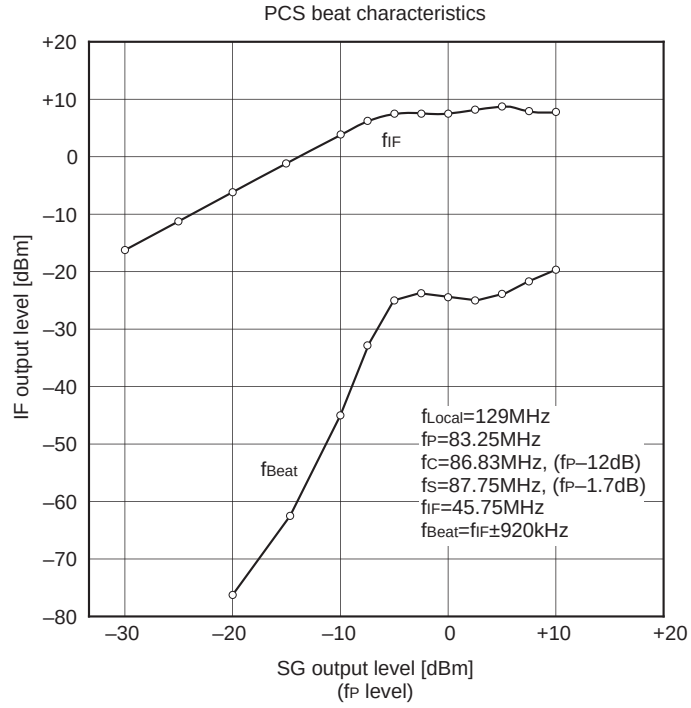
Next adjacent cross modulation vs. Reception frequency (Untuned input)



Oscillation frequency power supply fluctuation (PLL off)

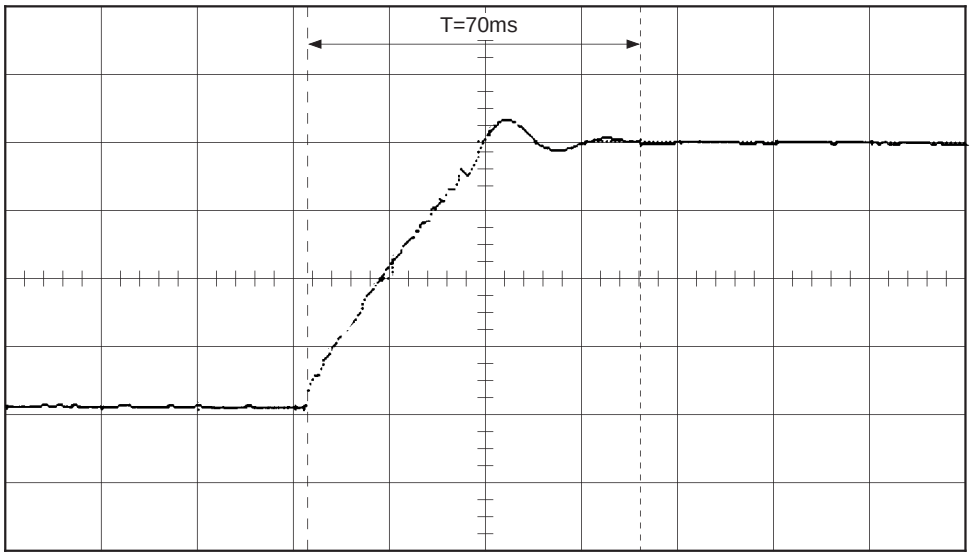


PCS beat characteristics



Tuning Response Time

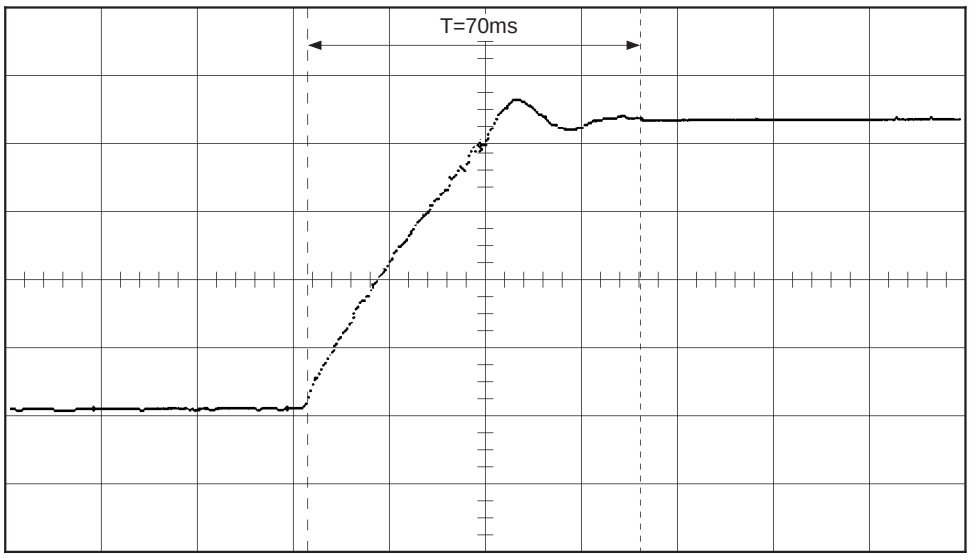
VHF (Low) 95MHz → VHF (High) 395MHz



5.0V/div
offset 10.0V

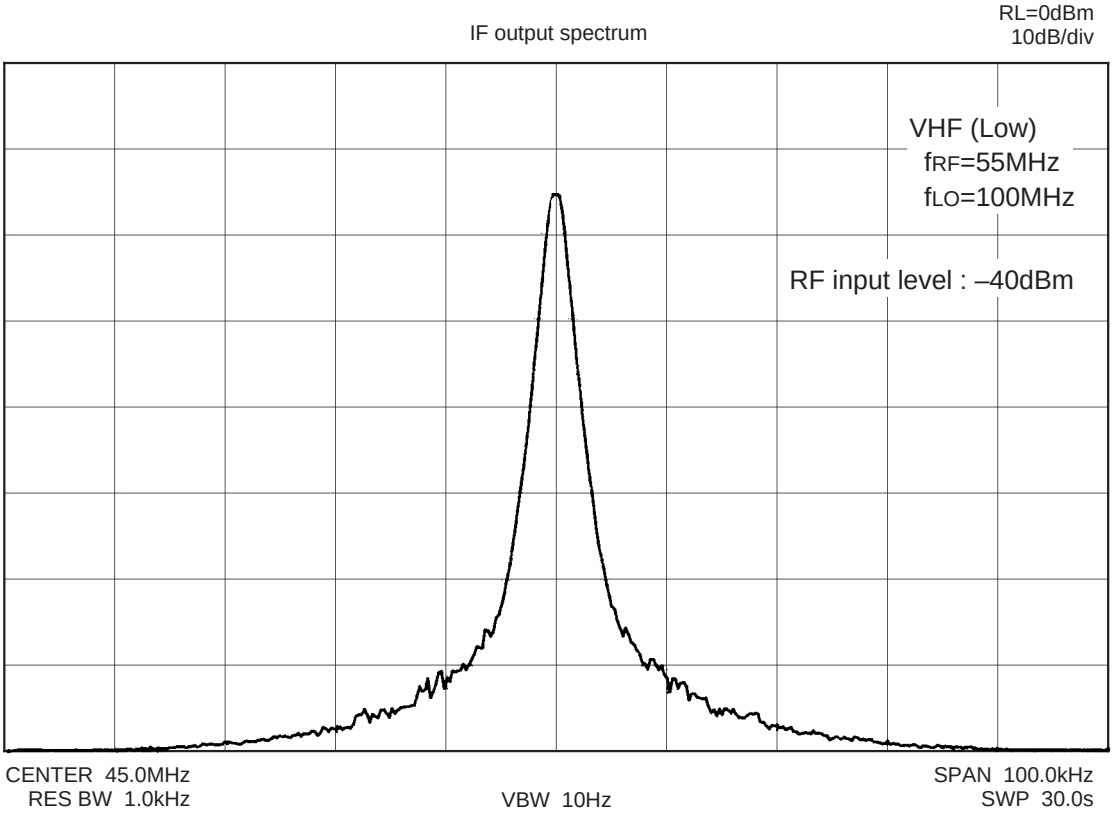
–90,0000ms 10,0000ms 110,000ms
20.0ms/div

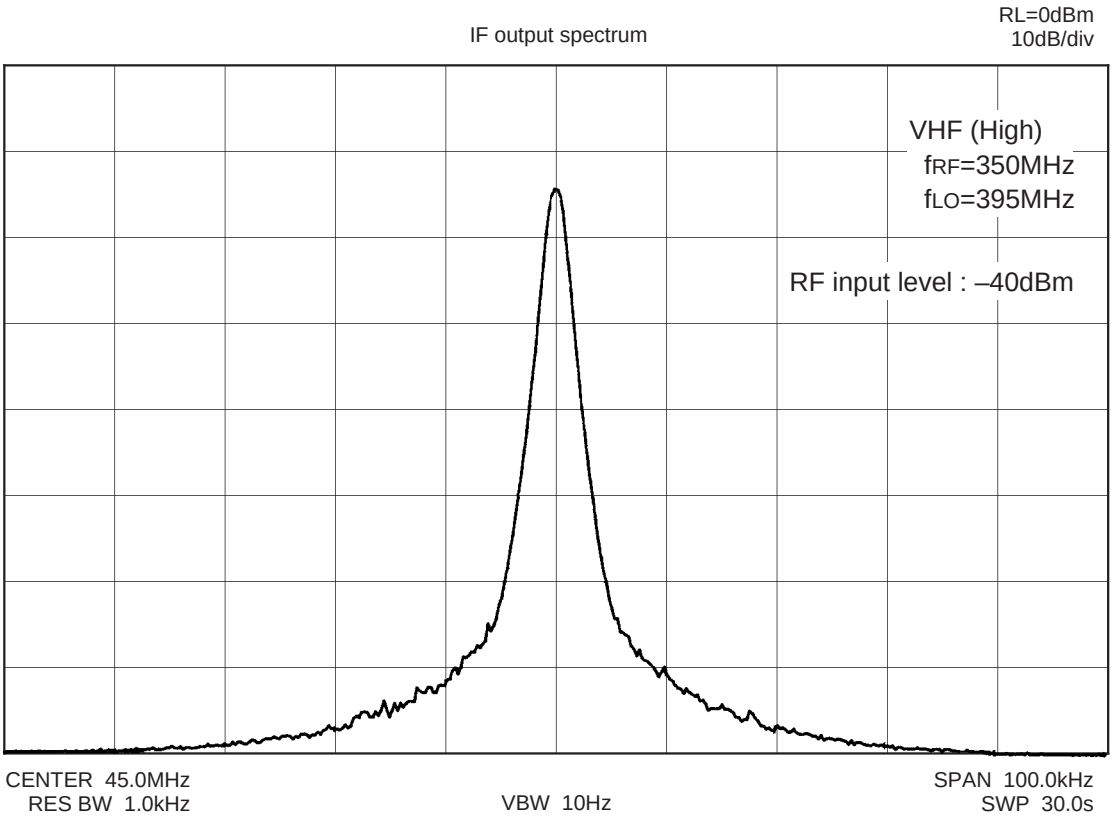
UHF 413MHz → UHF 847MHz

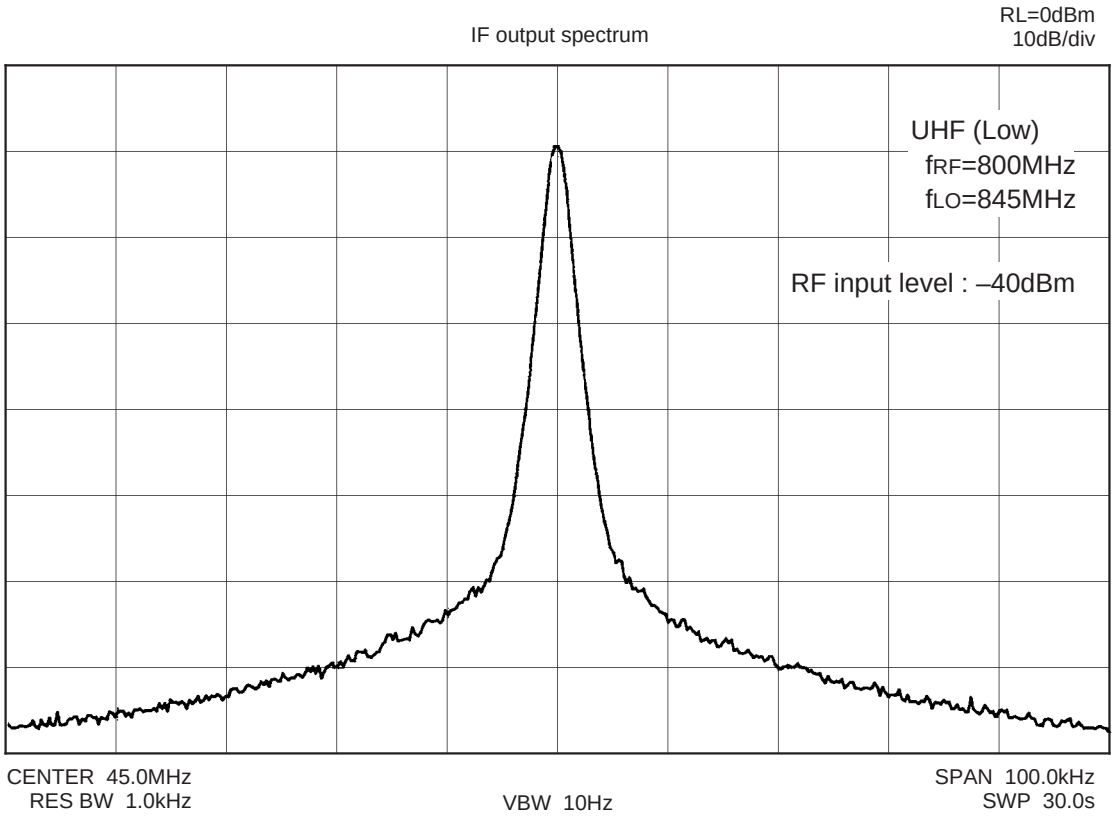


5.0V/div
offset 10.0V

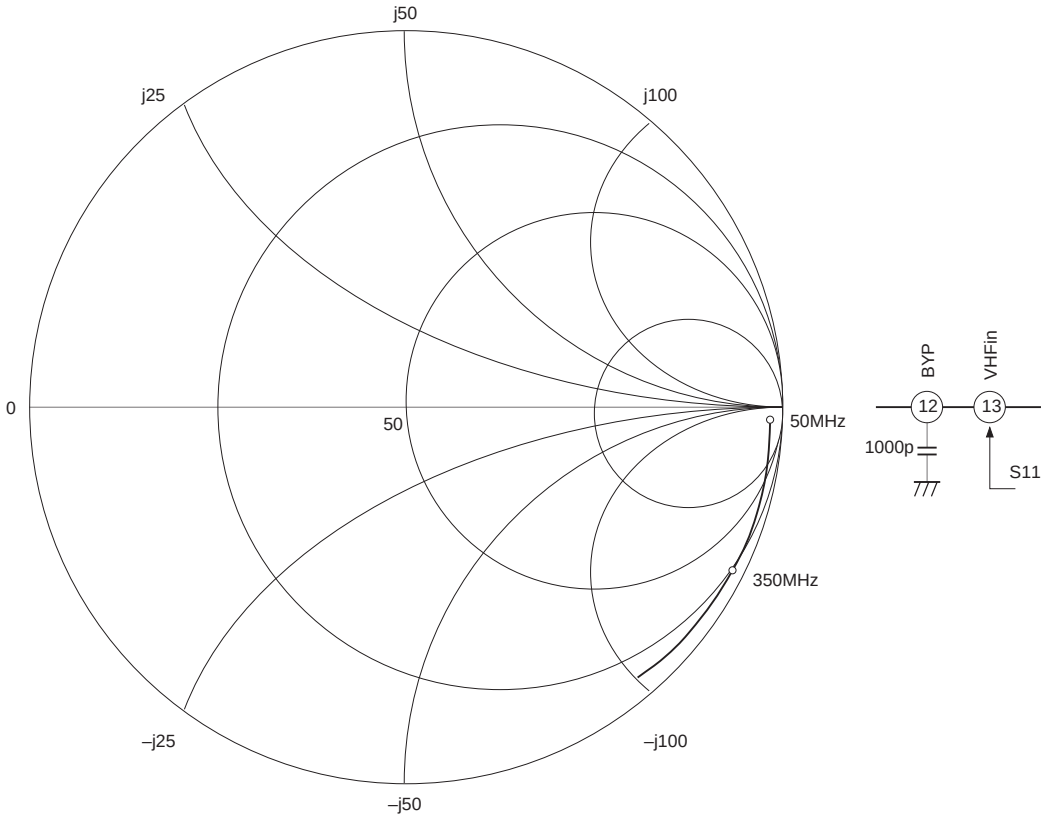
–90,0000ms 10,0000ms 110,000ms
20.0ms/div


IF output spectrum
RL=0dBm
10dB/div
VHF (Low)
fRF=55MHz
fLO=100MHz
RF input level : –40dBm
CENTER 45.0MHz
RES BW 1.0kHz
VBW 10Hz
SPAN 100.0kHz
SWP 30.0s

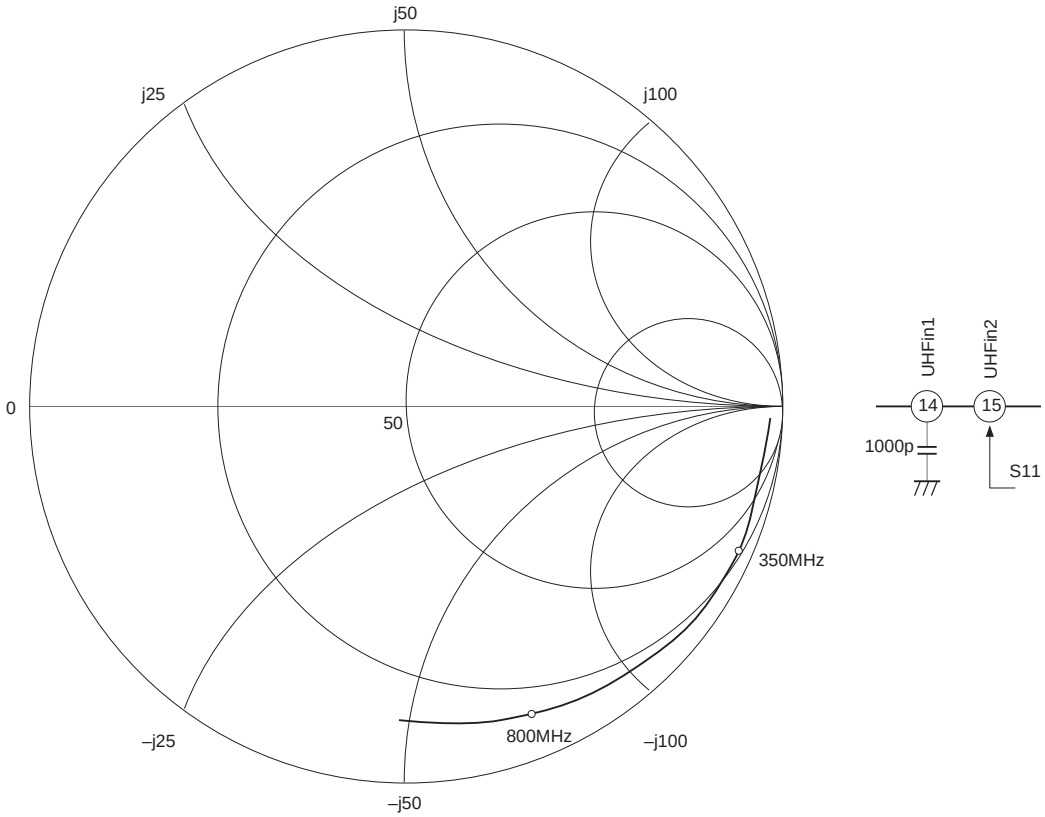

IF output spectrum
RL=0dBm
10dB/div
VHF (High)
fRF=350MHz
fLO=395MHz
RF input level : –40dBm
CENTER 45.0MHz
RES BW 1.0kHz
VBW 10Hz
SPAN 100.0kHz
SWP 30.0s


IF output spectrum
RL=0dBm
10dB/div
UHF (Low)
fRF=800MHz
fLO=845MHz
RF input level : –40dBm
CENTER 45.0MHz
RES BW 1.0kHz
VBW 10Hz
SPAN 100.0kHz
SWP 30.0s

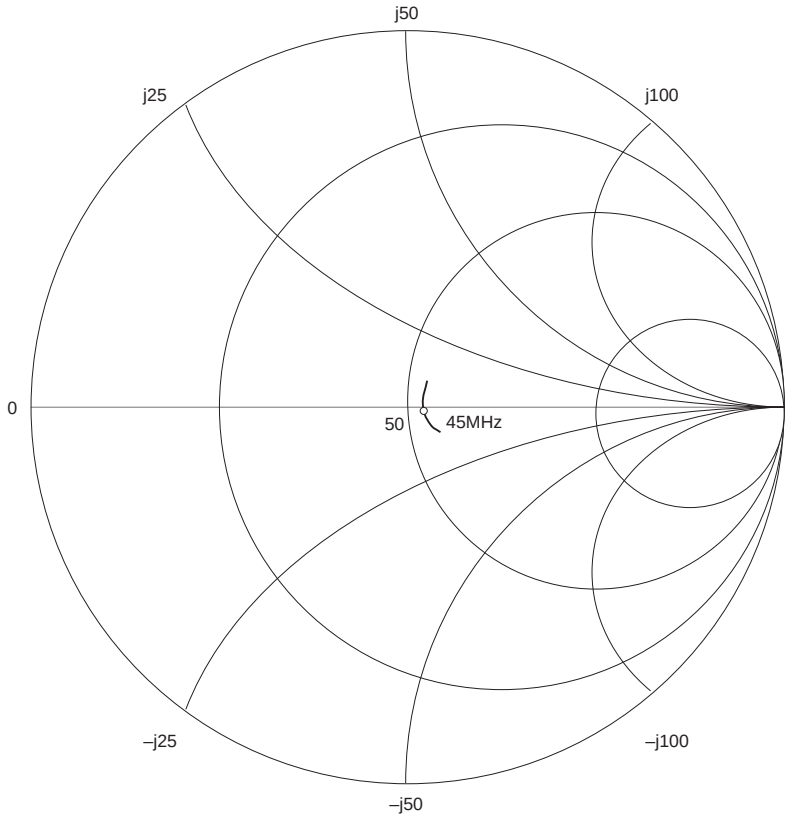
VHF Input Impedance



UHF Input Impedance

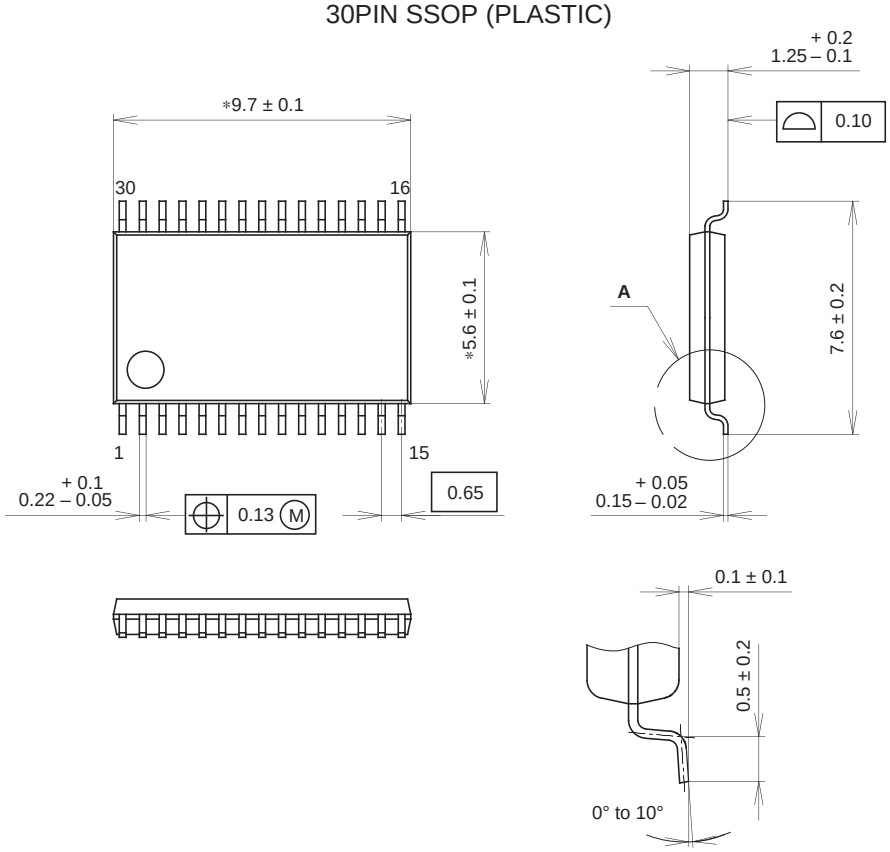


IF output Impedance



Package Outline Unit : mm

30PIN SSOP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

DETAIL **A**

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

SONY CODE	SSOP-30P-L01
EIAJ CODE	SSOP030-P-0056
JEDEC CODE	————